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CORDIC Based DCT for an Efficient Reconfigurable Architecture

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ABSTARCT: The demand for low power implementations of complex signal processing algorithms is increasing. For this purpose, Co-Ordinate Rotate Digital Computer (CORDIC) based 2-Dimensional Discrete Cosine Transform (2-D DCT) is used. In DCT all the computations are not equally important in generating the frequency domain outputs, by considering the importance difference in the DCT coefficients, the number of CORDIC iterations can be dynamically changed to efficiently balance the image quality and for low power consumption. Thus, the computational energy can be reduced without seriously compromising the image quality. The 2-D DCT process is decomposed into an 1-D DCT (row DCT) followed by another 1-D DCT (column DCT). The conventional CORDIC algorithm is designed to calculate cosine functions for the given angle and it is implemented in the reconfigurable architecture. The unique feature of this reconfigurable architecture is that it could be configured for the computation of a 32-point DCT or for parallel computation of two 16-point DCTs or four 8-point DCTs with a marginal control overhead. The reconfigurable architecture using CORDIC based 2D DCT can be constructed using HDL and the reconfigurable architecture is found to offer many advantages in terms of hardware complexity, regularity and modularity.

KEYWORDS:CORDIC DCT, Reconfigurable Architecture, Low power.

I. INTRODUCTION

With the explosive growth of multimedia services running on portable applications, the demand for low power implementations of complex signal processing algorithms is tremendously increasing. The most significant part of multimedia systems are the applications involving image and video processing, which are very computationally intensive and thus should be implemented with low cost because of the limited battery lifetime of portable devices. Many previous research efforts are focused on reducing power dissipation of image and video applications [7]–[8].Especially, low-power design of discrete cosine transform (DCT) [10] has been of particular interest, since DCT is one of the most computationally intensive operations in video and image compression, and it is widely adopted in many standards such as JPEG [2], MPEG [3], and H.264 [13]. Since first proposed in 1959 [1], Co-Ordinate Rotation Digital Computer (CORDIC) has been widely used to calculate the trigonometric functions in signal processing applications, such as QR decomposition [4], Fast Fourier transform [9], singular value decomposition [5], [6], and so on. Since CORDIC can be simply implemented with the iterative operations of additions and shifts, it has been widely used for the multiplierless low-power DCT architectures [15]–[20]. Many previous research works focused on reducing the hardware complexity of DCT such as Distribute Arithmetic (DA)-based DCT [11] and multiple constant multiplication (MCM)-based approach [12]. Although bit-serial DA-based approach offers a regular and simple DCT architecture, large hardware area is needed for bit-parallel operations because of additional ROMs and control logics. MCM-based DCT [12] can be simply implemented with a smaller number of shift and add operations, however, to make a trade-off between the image quality and computation energy, the computation sharing in different datapaths should be completely re-considered. For the low-power CORDIC-based DCT architecture presented in [16], data correlations between neighboring pixels are efficiently used to skip the internal CORDIC iterations. Approximation technique or incorporating compensation steps into the quantization is also exploited to reduce the power consumption of CORDIC-based DCT architecture [18]. Most of the previous research works are mainly focused on reducing the number of arithmetic units; the inherent data priorities in DCT coefficients, however, have not been exploited in the CORDIC-based DCT.

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In this paper we propose an architecture for approximate DCT of lengths N=8,16,32 using CORDIC based DCT. The proposed architecture is fully scalable, reconfigurable, and parallel architecture for approximate DCT computation. One uniquely interesting feature of the architecture is that it can be used for the computation of 32-point DCT which could be configured for parallel computation of
two 16-point DCTs or four 8-point DCTs. The proposed algorithm is found to be better than the existing methods in terms of power consumption and hardware complexity, as well.

II. CONVENTIONAL CORDIC BASED DCT ARCHITECTURE

The basic principal of CORDIC is to iteratively rotate avector using a rotation matrix [1], which is represented as follows:

$$\begin{bmatrix} x_i \\ y_i \\ z_i \end{bmatrix} = \begin{bmatrix} x_{i-1} - \sigma_i 2^{1-i} y_{i-1} \\ y_{i-1} - \sigma_i 2^{1-i} x_{i-1} \\ z_{i-1} - \sigma_i \propto_i \end{bmatrix} \quad (1)$$

where *x* and *y* are the vector coordinate components of *x* and *y* axes, respectively, *i* is the *i* th iteration step, *σ* is thesign-bit that can be +1 or −1 indicating the direction ofthe vector rotation, *z* is the accumulated rotation angle, and*α* is the predefined angle value of each microrotation step,$\alpha_i = \arctan(2^{1-i})$. In the CORDIC architecture, the amplitudeand argument of a given vector can be calculated using thevectoring mode, while the sine and cosine values of the givenangle are obtained with the rotation mode [14]. The hardwarearchitecture of the CORDIC iteration is shown in Fig. 1, whichis referred as a crossing-architecture.

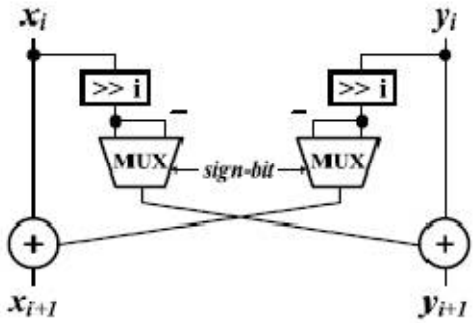

Fig. 1. Hardware architecture of CORDIC iteration.

In the CORDIC operation, the magnitude of the rotated vector is scaled and accumulated after every iteration according to the following equation:

$$Ki = \frac{1}{\sqrt{1+2^{2(1-i)}}} \quad (2)$$

After a series of iterations, the accumulated *Ki* value in (2) is converged to a constant as follows:

$$K(n) = \prod_{i=1}^{n} K\,i = \prod_{i=1}^{n} \frac{1}{\sqrt{1+2^{2(1-i)}}}$$

$$\Rightarrow \lim_{n \to \infty} K(n) \approx 0.60725 \quad (3)$$

where *n* is the number of iterations. The constant above is the scale-factor to restore the scaled magnitude of the rotated vector. The scale-factor is determined by the number of iterations. In the following sections, we use a low-power CORDIC architecture by modifying the number of iterations, where the vector rotates to the target angle in only one direction.

The 2-D DCT process is decomposed into an 1-D DCT (rowDCT) followed by another 1-D DCT (column DCT), which is expressed as the following equation:

$$Y = T\,xT^T = T\,(T\,x^T)^T \quad (3)$$

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where x and Y are 8 × 8 size of image data matrix and 2-D DCT transformed output matrix, respectively. T is the 8 × 8 1-D DCT basis matrix. The 2-D DCT process with separable 1-D DCT is shown in Fig. 2.

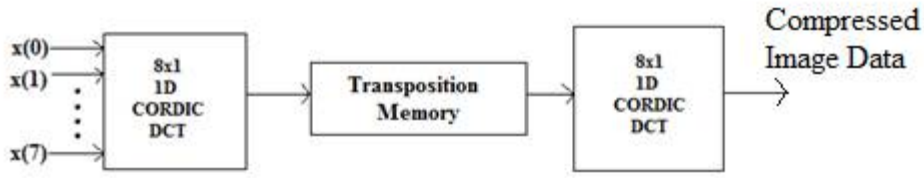

Fig. 2. 8 × 8 2-D DCT processor with separable 1-D DCT.

The 8 × 8 1-D DCT transform is expressed as

$$X(k) = c(k)/2 \sum_{x=0}^{7} x(i)\cos\left[\frac{(2i+1)k\pi}{16}\right] \quad (4)$$

where, K = 0,1, 2, ..., 7

$$c(k) = \begin{cases} \left(\frac{1}{\sqrt{2}}\right) & k = 0 \\ 1 & otherwise \end{cases}$$

where $x(i)$ is the input data, and $X(k)$ is 1-D DCT transformed output data. As a vector-matrix form, 1-D DCT is represented as $X = T\,x^T$, where T is the 8 × 8 DCT basis matrix. X and x are the output and input vectors, respectively. Since 8 × 8 DCT bases matrix T has a symmetric property, the 1-D DCT transform is represented as follows:

$$\begin{bmatrix} X(0) \\ X(4) \end{bmatrix} = 1/2 \begin{bmatrix} c_4 & c_4 \\ c_4 & -c_4 \end{bmatrix} \begin{bmatrix} x(0) + x(7) + x(3) + x(4) \\ x(1) + x(6) + x(2) + x(5) \end{bmatrix}$$

$$\begin{bmatrix} X(2) \\ X(6) \end{bmatrix} = 1/2 \begin{bmatrix} c_2 & c_6 \\ c_6 & -c_2 \end{bmatrix} \begin{bmatrix} x(0) + x(7) - x(3) - x(4) \\ x(1) + x(6) - x(2) - x(5) \end{bmatrix}$$

$$\begin{bmatrix} X(1) \\ X(3) \\ X(5) \\ X(7) \end{bmatrix} = 1/2 \begin{bmatrix} c_1 & c_3 c_5 & c_7 \\ c_1 & -c_7 - c_1 & -c_5 \\ c_5 & -c_1 & c_7 & c_3 \\ c_7 & -c_5 & c_3 & -c_1 \end{bmatrix} \begin{bmatrix} x(0) - x(7) \\ x(1) - x(6) \\ x(2) - x(5) \\ x(3) - x(4) \end{bmatrix} \quad (5)$$

where $c_k = \cos(k\pi/16)$. The cosine elements in (7) can bechanged into sine elements through trigonometric symmetric property, and (7) can be rearranged as the following equations:

$$\begin{bmatrix} X(0) \\ X(4) \end{bmatrix} = 1/2 \begin{bmatrix} c_4 & -s_4 \\ s_4 & c_4 \end{bmatrix} \begin{bmatrix} x(0) + x(7) + x(3) + x(4) \\ x(1) + x(6) + x(2) + x(5) \end{bmatrix}$$

$$\begin{bmatrix} X(2) \\ X(6) \end{bmatrix} = 1/2 \begin{bmatrix} c_6 & -s_6 \\ s_6 & c_6 \end{bmatrix} \begin{bmatrix} x(0) + x(7) - x(3) - x(4) \\ x(1) + x(6) - x(2) - x(5) \end{bmatrix}$$

$$\begin{bmatrix} X(1) \\ X(7) \end{bmatrix} = 1/2 \begin{bmatrix} c_7 & s_7 \\ -s_7 & c_7 \end{bmatrix} \begin{bmatrix} x(3) - x(4) \\ x(0) - x(7) \end{bmatrix} + 1/2 \begin{bmatrix} c_3 & s_3 \\ -s_3 & c_3 \end{bmatrix} \begin{bmatrix} x(1) - x(6) \\ x(2) - x(5) \end{bmatrix}$$

$$\begin{bmatrix} X(3) \\ X(5) \end{bmatrix} = 1/2 \begin{bmatrix} c_3 & -s_3 \\ s_3 & c_3 \end{bmatrix} \begin{bmatrix} x(0) - x(7) \\ x3 - x(4) \end{bmatrix} - 1/2 \begin{bmatrix} c_1 & s_1 \\ -s_1 & c_1 \end{bmatrix} \begin{bmatrix} x(2) - x(5) \\ x(1) - x(6) \end{bmatrix} \quad (6)$$

where $s_m = \sin(m\pi/16) = ck$, and $m = 8-k$. The rearranged1-D DCT equation is now represented as vector rotation matrix together with the consecutive CORDIC iterations as shown in Fig. 3.

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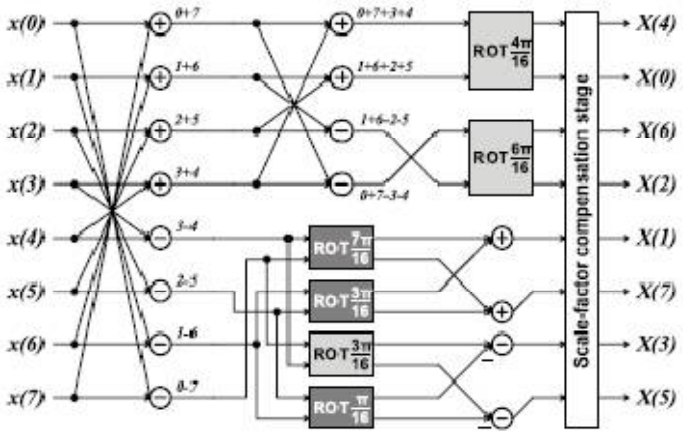

Fig. 3. Hardware architecture of CORDIC-based 1-D DCT.

Now, DCT can be implemented using only shifters andadders without multiplier [15]. Please note that the sign-bits and the scale-factor are known ahead since the input angles of CORDIC module are given as the DCT bases.

III. SCALABLE AND RECONFIGURABLE ARCHITECTURE FOR DCT COMPUTATION

DCT ofdifferent lengths such as N=8, 16, 32 are required to be used in video coding applications. Therefore, a given DCT architecture should be potentially reused for the DCT of different lengths instead of using separate structures for different lengths. We propose here such reconfigurable DCT structures which could be reused for the computation of DCT of different lengths.A reconfigurable design for the computation of N=32-, 16-, and8-point DCTs is presented in Fig. 4.

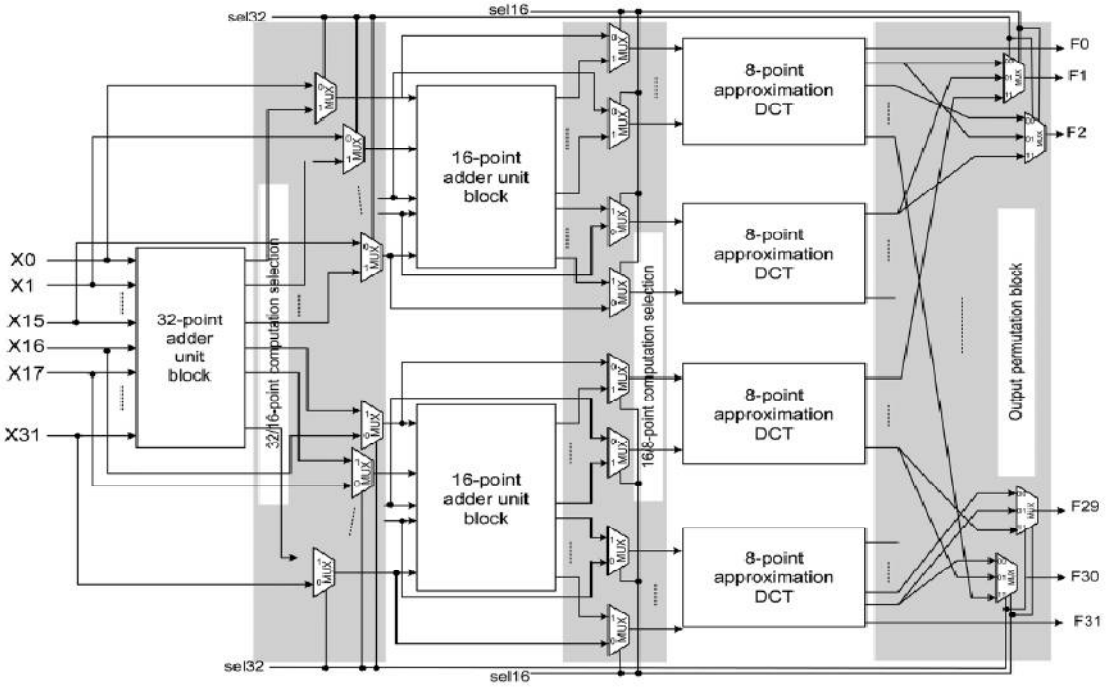

Fig. 4. Proposed reconfigurable architecture for approximate DCT of lengths N=8 ,16 and 32.

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It performs the calculationof a 32-point DCT or two 16-point DCTs in parallel or four 8-point DCTs in parallel. The architecture is composed of 32-point input adder unit, two 16-point input adder units, and four 8-point DCT units which is the CORDIC based DCT unit. The reconfigurability is achieved by three control blocks composed of 64 2:1 MUXes along with 30 3:1 MUXes. The first control block decides whether the DCT size is of 32 or lower. If Sel 32=1, the selection of input datais done for the 32-point DCT, otherwise, for the DCTs of lower lengths. The second control block decides whether the DCT size is higher than 8. If Sel 16=1, the length of the DCT to be computed is higher than 8 (DCT length of 16 or 32), otherwise, the length is 8. The third control block is used for the output permutation unit which re-orders the output depending on the size of the selected DCT. Sel 32 and Sel 16 are used as control signals to the 3:1 MUXes. Specifically, for $\{\text{Sel 32, Sel 16}\}_2$ equal to {00}, {01} or {11} the 32 outputs correspond to four 8-point parallel DCTs, two parallel 16-point DCTs, or 32-point DCT, respectively. Note that the throughput is of 32 DCT coefficients per cycle irrespective of the desired transform size.

IV. RESULTS AND DISCUSSIONS

The experimental results of the proposed CORDIC based DCT architecture is presented. The number of CORDIC iterations are decided according to the target PSNR of 31.5 dB. For comparisons various DCT architectures such as DA-based DCT [11], MCM [12] and CORDIC-based Loeffler DCT [18] are used and tabulated in Table I.

Table I
Comparison Result for Various DCT Architectures

Architecture	DA-Based DCT	MCM	CORDIC-Based Loeffler DCT	Proposed
PSNR (dB)	31.63	31.49	30.61	31.45
Power (mW)	6.76	5.42	6.54	5.11

(a) (b) (c)

Fig.5 Lena images obtained using the (a) proposed reconfigurable CORDICbasedDCT. (b) CORDIC based Loeffler DCT. (c) DA based DCT.

V. CONCLUSION

Thus the proposed Reconfigurable DCT Architecture using CORDIC gives a low power architecture with minimal image degradation and it can assist the low power design of image and video compression applications. In this architecture, the computation of 32-point DCT could be configured for parallel computation of two 16-point DCTs or four 8-point DCTs. DCT of length N could be derived from a pair of DCTs oflength (N/2) at the cost of N additions for input pre-processing. The proposed approximated DCT has several advantages, such as of regularity, structural simplicity, lower-computational complexity, and scalability.

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